

INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>	Docket Number (Optional) BUR920010040US1(145	Application Number Unassigned
	Applicant(s) Jeffrey P. Gambino, et al.	
	Filing Date Herewith	Group Art Unit Unassigned

U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
		6,180,501	01/30/01	Pey, et al.			
		6,174,794	01/16/01	Gardner, et al.			
		6,140,191	10/31/00	Gardner, et al.			
		6,077,745	06/20/00	Burns, Jr., et al.			
		6,033,957	03/07/00	Burns, Jr., et al.			
		5,739,057	04/14/98	Tiwari, et al.			
		5,646,058	07/08/97	Taur, et al.			
		5,574,294	11/12/96	Shepard			
		5,963,800	10/1999	Augusto			
		6,004,837	12/1999	Gambino et al.			

FOREIGN PATENT DOCUMENTS								
	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
		11-186557	07/09/99	Japan				

OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>	
	Chang, L., "Industrial Planar FinFET Fabrication Using Standard Processing Tools," (last modified February 21, 2001), p. 1, < http://hera.berkeley.edu/IRO/Summary/01abstracts/leland.2.html >
	Choi, Y., et al., "Asymmetrical Double Gate FinFET," (last modified February 21, 2001) p.1, < http://buffy.eecs.berkeley.edu/IRO/Summary/00abstracts/ykchoi.2.html >

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.